ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT, OAKLAND UNIVERSITY ECE-2700: Digital Logic Design

Student Honor Pledge:

All work submitted is completed by me directly without the use of any unauthorized resources or assistance Initials:

Quiz 2

(October 12th @ 5:30 pm)

PROBLEM 1 (40 PTS)

Complete the following table:

REPRESENTATION			
Decimal	Sign-and-magnitude	1's complement	2's complement
		1111	
		01000	
	010111		
-10			

Convert the following decimal number to its 2's complement representation: -10.25 (5 pts)

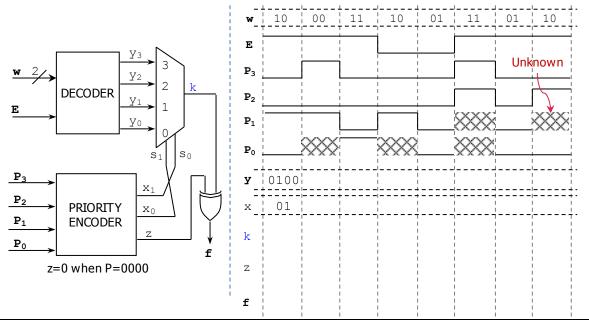
PROBLEM 2 (20 PTS)

Perform the following operation in the 2's complement system, i.e., provide the summands and the result in 2's complement • representation (indicate the carries). Use the minimum number of bits to represent both the summands and the result so that the overflow bit is 0.

~ -17 + 10

PROBLEM 3 (40 PTS)

• Complete the timing diagram of the circuit shown below: $y = y_3 y_2 y_1 y_0$, $x = x_1 x_0$



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